#8 CE 8/9/01

Attorney's Docket No.: 042390.P5549 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
Bogin et al.	Examiner: Elmore, R.
Application Number: 09/205,086	Art Unit 2187
Filed: December 4, 1998	
For: Method and Apparatus for Self Timing Refresh	

Assistant Commissioner of Patents
Washington, D.C. 20231

DECLARATION UNDER 37 CFR 1.131 IN SUPPORT OF PRIOR INVENTION

We, Zohar Bogin, David D. Lent and Vincent Von Bokern declare:

1. We are the inventors of the claims of the above-captioned patent application ("the Application") and the inventors of the subject matter described therein.

2. At least prior to June 4, 1998, the filing date of U.S. Patent No. 6,134,167 cited in an Office Action mailed July, 17, 2001 the invention caimed in the Application had been conceived in the United States.

3. The invention was actually reduced to practice prior to June 4, 1998.

4. Attached Exhibit A, dated June 11, 1997, is a redacted system design presentation describing the design of the mechanism for self timing refresh and establishes that

the subject matter claimed in the Application had been conceived in the United States prior to November 3, 1998.

We further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application of any patent issuing thereon.

Dated: 7, 26, 2001 — Zohar Bogin

Zohar Bogin

Dated: July 26, 2001 — David D. Lent

David D. Lent

Dated: July 27, 2001 — Vincent E. Von Bokern

Vincent Von Bokern

440BX W-unit MAS update
6/11/97

Overview

This document describes changes to the W-unit resulting from introduction of the BXPWROK pin to reset resume logic as early as possible in the power-up sequence. The intent of this change is to avoid driving the DRAM interface to unknown states during power-up prior to the rising edge of SUS_STAT#.

The key changes are:

1) "Resume" logic is reset immediately as 440BX gets a stable power supply, rather than remaining uninitialized until SUS_STAT# rising edge which occurs 32 us before PCIRST#.
2) SUSCLK is deleted in order for the pin to be used as BXPWROK. Therefore, the ring oscillator must be used to time refresh periods during suspend.
3) To compensate for speed variations in the oscillator, an auto-calibration mechanism is included which will measure the number of oscillator clocks in a refresh period during normal operation, and store this value as the number of oscillator clocks to count during suspend.

Implementation

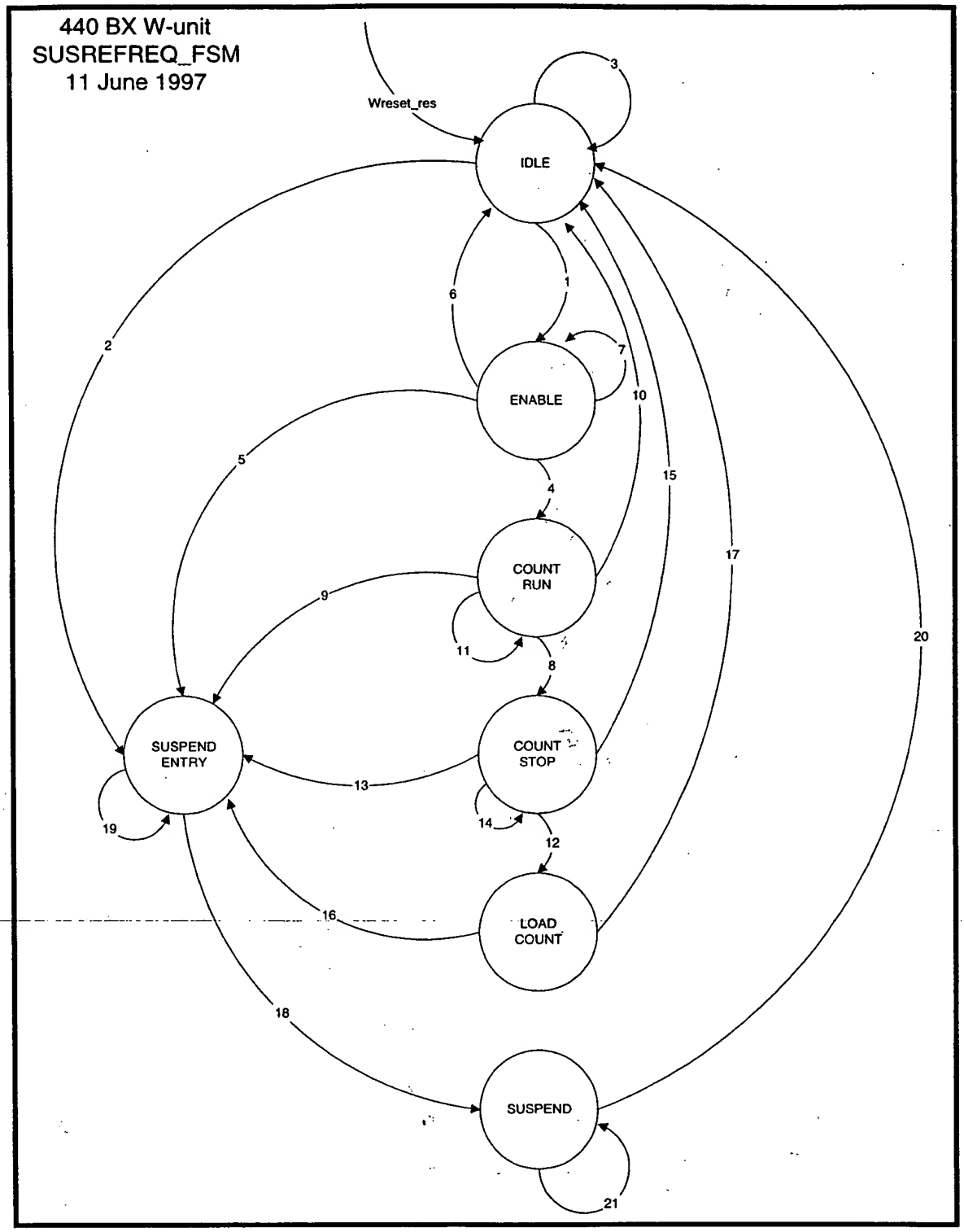
Reset Logic Changes:

Wreset_res, which resets "resume logic" which is only reset during cold boot, is driven active upon sampling BXPWROK inactive. It is deasserted synchronously from sampling PCIRST# inactive, and is then remains deasserted until BXPWROK is again sampled inactive.

Suspend Refresh Control:

Logic added for suspend refresh control includes a new state machine which controls a 12 bit counter. The state machine runs on rSCLK while the counter runs on oscclk. The state machine (susrefreq_fsm) identifies three operating windows—idle, counting oscclks for auto-calibrate, or counting oscclks to generate refresh requests during suspend. In addition to identifying these windows, the state machine has wait states to allow synchronization of communication between itself and the oscclk counter.

EXHIBIT A


440 BX W-unit
SUSREFREQ_FSM
11 June 1997
Wreset_res
IDLE
ENABLE
COUNT RUN
SUSPEND ENTRY
COUNT STOP
LOAD COUNT
SUSPEND
1
2
3
4
5
6
7
8
9
10
11
12
13
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STATE	DESCRIPTION
IDLE	FSM stays here if SDRAM, or if auto-calibrate is disabled and not in suspend mode count_clr = '1', count_run = '0'
ENABLE	Waiting for a B refresh timer time-out to begin auto-calibrate oscclk counting count_clr = '0', count_run = '0'
COUNT_RUN	Counting oscclks for auto-calibrate count_clr = '0', count_run = '1'
COUNT_STOP	Done counting oscclks, waiting for counter to recognize that the oscclk synchronized version of count_run inactive to ensure that a stable value is presented to H-unit for loading. count_clr = '0', count_run = '0'
LOAD_COUNT	Count value for auto-calibrate is stable, pulse WHload_srr to load into H-unit register count_clr = '0', count_run = '0'
SUS_ENTRY	Entering suspend, clearing counter and waiting for clear indication to be recognized in the oscclk domain count_clr = '1', count_run = '0'
SUSPEND	In suspend refresh mode, running the counter to track when a refresh period has elapsed. Counter is cleare refresh request asserted to sfreq machine in wcrasgn to perform oscclk based CBR refresh (or enter EDO s refresh mode) count_clr = '0', count_run = '0'

Arc Table

FROM	TO	CONDITION
IDLE	IDLE	!(IDLE to ENABLE or SUS_ENTRY)
IDLE	ENABLE	SCRR auto adjust bit enabled, counter clear active has been recognized in oscclk domai DRAM is populated with EDO
IDLE	SUS_ENTRY	SUS_STAT# has been sampled active, conditions for W-unit to take over DRAM interf been met (DRAM idle, refresh queue empty), and DRAM is populated with EDO
ENABLE	IDLE	SCRR auto adjust bit disabled
ENABLE	SUS_ENTRY	SUS_STAT# has been sampled active, conditions for W-unit to take over DRAM interf been met (DRAM idle, refresh queue empty)
ENABLE	RUN_COUNT	B-unit refresh counter timed out
ENABLE	ENABLE	!(ENABLE to IDLE, SUS_ENTRY, or RUN_COUNT)
RUN_COUNT	IDLE	SCRR auto adjust bit disabled
RUN_COUNT	SUS_ENTRY	SUS_STAT# has been sampled active, conditions for W-unit to take over DRAM interf been met (DRAM idle, refresh queue empty)
RUN_COUNT	STOP_COUNT	B-unit refresh counter timed out
RUN_COUNT	RUN_COUNT	!(RUN_COUNT to IDLE, SUS_ENTRY, or STOP_COUNT)
STOP_COUNT	IDLE	SCRR auto adjust bit disabled
STOP_COUNT	SUS_ENTRY	SUS_STAT# has been sampled active, conditions for W-unit to take over DRAM interf been met (DRAM idle, refresh queue empty)
STOP_COUNT	LOAD_COUNT	counter run inactive has been recognized in oscclk domain
STOP_COUNT	STOP_COUNT	!(STOP_COUNT to IDLE, SUS_ENTRY, or LOAD_COUNT)
LOAD_COUNT	SUS_ENTRY	SUS_STAT# has been sampled active, conditions for W-unit to take over DRAM interf been met (DRAM idle, refresh queue empty)
LOAD_COUNT	IDLE	!(LOAD_COUNT to SUS_ENTRY)
SUS_ENTRY	SUSPEND	counter clear active has been recognized in oscclk domain
SUS_ENTRY	SUS_ENTRY	!(SUS_ENTRY to SUSPEND)
SUSPEND	IDLE	Resume sequence has been completed and control of DRAMs has been transferred from back to D-unit
SUSPEND	SUSPEND	!(SUSPEND to IDLE)